UTKALMANI GOPABANDHU INSTITUTE OF ENGINEERING, ROURKELA

LESSON PLAN

SESSION: 2025-2026

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

SUBJECT CODE: Th.3

NAME OF THE SUBJECT: DIGITAL ELECTRONICS

BRANCH: ELECTRONICS & TELECOMMUNICATION

SEMESTER: DIPLOMA 3rd SEM

NUMBER OF CLASSES ALLOTED PER WEEK : 3

TOTAL PERIODS ALLOTED TO THE SUBJECT ACCORDING TO SCTEVT: 45

NAME OF THE FACULTY: MANASI PRIYADARSHINI

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SEMESTER: DIPLOMA -III

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NO OF CLASSES ALLOTTED PER WEEK: 3 (14/07/2025 to 15/11/2025)

Week/Date	Lecture	Topic to be covered
1st week	1st	**UNIT-1** **Logic Gates** 1.1 Basic logic gates: OR, AND, and NOT 1.1.1 Truth tables 1.1.2 Logic symbols 1.1.3 Logic voltage levels 1.1.4 Logic circuit design examples
	2nd	1.2Integrated Circuits 1.3NOR, NAND, Exclusive OR, and Exclusive NOR gates. 1.4NOR and NAND gates used as inverters
	3rd	1.5Fan-in and fan-out 1.6Termination of unused inputs
2nd week	1st	1.7 AND and OR gates constructed from NAND and NOR gates
	2nd	**UNIT-2** **Boolean Algebra** 2.1 Boolean operations (OR, AND, NOT) 2.2 Representation of logic circuits by Boolean expressions.

	3rd	2.3 Laws of Boolean algebra: Double inversion: A"=A OR identities: A+0 = A, A+1=1, A+A=A, A+A'=1 AND identities: A.0=0, A.1=A, A.A=A, A.A'=0 Cumulative laws: A+B=B+A, A.B=B.A Associative laws:(A+B)+C=A+(B+C), (A.B).C=A.(B.C) Distributive laws: A+(B.C)=(A+B).(A+C), A.(B+C)=A.B+A.C
3rd week	1st	DeMorgan's theorems:(A+B+C+...)'=A'.B'.C'...,(A.B.C...)'=A'+B'+C'... Applications to logic circuit simplifications and design 2.4 Equivalent logic gates 2.5 NAND and NOR implementations of logic circuits.
	2nd	2.6 Standard forms of Boolean expressions 2.6.1 Sum-of-products (SOP)
	3rd	2.6.2 Product-of-sums (POS)

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4th week	1st	2.7 Karnaugh mapping(K MAP)
	2nd	K-map CONTINUED
	3rd	K MAP CONTINUED
5th week	1st	**UNIT-3** **Combinational Logic Circuits** 3.1 Half adder 3.2 Full adder
	2nd	3.3Half Subtractor 3.4 Full Subtractor
	3rd	3.5 :4 bit adder. 3.6:Multiplexer (4:1)

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6th week	1st	3.7:De- multiplexer (1:4) 3.8:Decoder
	2nd	3.9: Encoder 3.10: Digital comparator (3 Bit)
	3rd	Digital comparator (3 Bit) continued
7th week	1st	3.11:Seven segment Decoder
	2nd	**UNIT-4:** **Latches & Flip-Flops** 4.1. Basic latches 4.1.1 NOR latch 4.1.2 NAND latch 4.1.3 Example uses of latches
	3rd	4.1. Gated latches 4.1.1 Gated S-R latch 4.1.2 Gated D-latch

8th week	1st	4.1. Flip-flops: 4.1.1 Master-slave and edge-triggered principles 4.1.2 S-R flip-flop
	2nd	4.1.1 D-type flip-flop
	3rd	4.1.1 J-K flip-flop 4.1.2 T-type flip-flop Flip-flop timing diagrams

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10th week	1st	**UNIT-5:** **COUNTERS** Circuit diagram and working principle of Binary counters
	2nd	up-down counter (circuits, truth tables, and timing diagrams) Asynchronous counters and ripple counter
	3rd	Synchronous counters Decade counter
11th week	1st	Module–n counter and its combinations Divide-by-n counters obtained from truncated binary sequences
	2nd	Synchronous counter design using D-type flip-flops
	3rd	Synchronous counter design using J-K flip- flops

12th week	1st	**UNIT-6:** **SHIFT REGISTERS** Circuit diagram, truth tables, and timing diagrams of Shift Registers Serial input shift register
	2nd	Serial/parallel load shift register
	3rd	6.1 Shift register counters Ring counter

13th week	1st	Self- starting ring counter
	2nd	Johnson counter 7.1 Define the terms ROM, RAM, PROM, EPROM. 7.2 Draw a typical memory cell 7.3 Design a small diode matrix ROM to serve as a code converter. 7.4 Design and draw the logic diagram of a specified size memory system 7.5 Operating principle of dynamic memory 7.6 Advantages and disadvantages of dynamic memory vs. static memory Difference between dynamic memory vs. static memory
	3rd	**UNIT-7:** **SEMICONDUCTOR MEMORIES** Define the terms ROM, RAM, PROM, EPROM
14th week	1st	Draw a typical memory cell Design a small diode matrix ROM to serve as a code converter
	2nd	Design and draw the logic diagram of a specified size memory system
	3rd	Operating principle of dynamic memory
15th Week	1st	Advantages and disadvantages of dynamic memory vs. static memory Difference between dynamic memory vs. static memory
	2nd	**UNIT-8:** **SEQUENTIAL CIRCUIT DESIGN** Combinational vs. Sequential circuits
	3rd	Adder
16th Week	1st	Subtractor
	2nd	decoder
	3rd	multiplexer
17th Week	1st	de-multiplexer
	2nd	comparator
	3rd	Finite state machines- Concept only
18th Week	1st	Short question discussion
	2nd	Long question discussion
	3rd	VST(ALL CHAPTER)