

UTKALMANI GOPABANDHU INSTITUTE OF
ENGINEERING, ROURKELA



LESSON PLAN

SESSION: 2023-2024

DEPARTMENT OF ELECTRONICS AND
TELECOMMUNICATION ENGINEERING

SUBJECT CODE: Th.3

NAME OF THE SUBJECT: DIGITAL ELECTRONICS

BRANCH: ELECTRONICS & TELECOMMUNICATION

SEMESTER: DIPLOMA 3rd SEM

NUMBER OF CLASSES ALLOTTED PER WEEK : 4

**TOTAL PERIODS ALLOTTED TO THE SUBJECT ACCORDING TO
SCTEVT: 60**

NAME OF THE FACULTY: MANASI PRIYADARSHINI

UTKALMANI GOPABANDHU INSTITUTE OF ENGINEERING,ROURKELA



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SUBJECT CODE: Th.3
NAME: DIGITAL ELECTRONICS
BRANCH: ELECTRONICS & TELECOMMUNICATION
SEMESTER: DIPLOMA -III
PERIODS PER WEEK: 4
NAME OF THE FACULTY: MANASI PRIYADARSHINI
NO OF CLASSES ALLOTTED PER WEEK : 4(01/08/2023 to 30/11/2024)

Week/Date	Lecture	Topic to be covered
1 st week	1 st	Chapter-1 Introduction to digital electronics
	2 nd	Number system
	3 rd	Interconversion of number systems Binary arithmetic operation
2 nd week	1 st	1's & 2's complement
	2 nd	Subtraction using 1'S and 2'scomplement
	3 rd	Codes, BCD code
	4 th	Ex-3, gray, alphanumeric codes
3 rd week	1 st	Logic gates
	2 nd	Universal gates
	3 rd	Boolean algebra
	4 th	DeMorgan's theorem

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4 th week	1 st	Minterm and Maxterm
	2 nd	k-map (2 & 3 variable)
	3 rd	4-variable k-map
	4 th	Don't care condition, problem
5 th week	1 st	Combinational logic circuit, halfadder and full adder
	2 nd	Half Subtractor and full subtractor
	3 rd	Parallel adder, serial adder(4 bit binary adders)
	4 th	Multiplexer (4:1) mux
6 th week	1 st	Multiplexer application
	2 nd	Demultiplexer
	3 rd	Encoder
	4 th	Decoder

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7 th week	1 st	Digital magnitude comparator
	2 nd	3-bit magnitude comparator
	3 rd	Seven segment decoder
	4 th	Sequential logic circuit
8 th week	1 st	Latch
	2 nd	S-R Flip-flop
	3 rd	J-K flip-flop
	4 th	Race-around condition
9 th week	1 st	T flip-flop
	2 nd	Application of flip-flop
	3 rd	Registers
	4 th	SISO shift register

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10 th week	1 st	Registers, SIPO shift register, PISO shift register
	2 nd	Universal shift register
	3 rd	Types of counters and counter application
	4 th	Binary Counters and asynchronous ripple counter (up and down)
11 th week	1 st	Decade counter
	2 nd	Synchronous counter
	3 rd	Design of asynchronous counter
	4 th	Ring counter
12 th week	1 st	RAM, ROM, STATIC RAM, DYNAMIC RAM
	2 nd	Logic families
	3 rd	Characteristics of digital ICs
	4 th	Transistor-transistor logic

13 th week	1 st	CMOS logic
	2 nd	Introduction to ADC
	3 rd	Introduction to DAC
	4 th	Weighted-resistor type DAC
14 th week	1 st	R-2R ladder type DAC
	2 nd	Basic principle of ADC
	3 rd	Counter type ADC
	4 th	Successive approximation type ADC
15 th Week	1 st	Chapter wise long question and short question discussion
	2 nd	Semester Question discussion
	3 rd	VST(1 ST CHAPTER)
	4 th	VST(2 ND CHAPTER)
16 th Week	1 st	VST(3 RD CHAPTER)
	2 nd	VST(4 TH CHAPTER)
	3 rd	VST(5 TH CHAPTER)
	4 th	VST(6 TH CHAPTER)
17 th Week	1 st	VST(7 TH CHAPTER)
	2 nd	VST(8 TH CHAPTER)
	3 rd	VST(ALL CHAPTER)
	4 th	VST(ALL CHAPTER)
18 th Week	1 st	VST(ALL CHAPTER)
	2 nd	VST(ALL CHAPTER)
	3 rd	VST(ALL CHAPTER)
	4 th	VST(ALL CHAPTER)